IN THE SPECIFICATION:

Please replace the paragraph beginning on page 6, line 17 with the following amended paragraph:

to page 7, line 13, with the following rewritten paragraphs:

--Referring now to Fig. 4, there is shown a cross-sectional view of a memory device including a CAM cell in a peripheral circuit region and a flash memory in a cell region according to the present invention.

Please replace the paragraph beginning on page 6, line 19 with the following amended paragraph:

--A tunnel oxide layer TO and a floating gate F are formed in a cell region of a semiconductor substrate 21. The floating gate F is formed with a first polysilicon layer. A gate insulating film 22 ~~in which~~ including an oxide film and a nitride film ~~are stacked is~~ formed on a semiconductor substrate and the floating gate F ~~21~~. For example, the gate insulating film 22 has a second oxide film 22C, a nitride film 22B and a first oxide film 22A, which are sequentially stacked on the semiconductor ~~device~~ substrate 21. The gate insulating film 22 is used as a dielectric film formed between the floating gate and the control gate in the process of manufacturing a flash memory cell. At this time, the thickness of the gate insulating film 22 is in the range of 30 ~300Å. For example, the gate insulating film 22 of a three layer has the first oxide film 22A, the nitride film 22B and the second oxide film 22C each of which has the thickness of 10 ~100Å. Meanwhile, the gate insulating film 22 may be formed using a stack

structure of a first oxide film, a first nitride film. a second oxide film and a second nitride film, a stack structure of the first oxide film, the first nitride film, the second oxide film, the second nitride film and the third oxide film, and the like, as well of the stack structure of the first oxide film 22A, the nitride film 22B and the second oxide film 22C. Also, after forming a second polysilicon film ~~23~~ on the gate insulating film 22, the second polysilicon film ~~23~~ and the gate insulating film 22 are patterned ~~to form a gate~~. Thus, a gate 23 of an address memory is formed in the peripheral circuit region while a control gate C of the flash memory is formed in the cell region from the second polysilicon layer. And also, the gate insulating is left between the semiconductor substrate 21 and the gate 23 and between the floating gate F and the control gate C. A source region 24 and a drain region 25 are formed on the semiconductor substrate 21 by means of impurity ion implantation process.--